REMARKS

Reconsideration of this application is respectfully requested. Claims 5, 7, 13, 15, 20, and 26 stand rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 27, 29, 30, and 32 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent Number 6,577,156 by Anand et al. (hereinafter "Anand"). Claims 1-21, 27, 28, 30, 31, 35, and 37 stand rejected under 35 U.S.C. § 103(a) as being anticipated by U.S. Patent Number 6,249,465 by Weiss et al. (hereinafter "Weiss"), in view of Anand. Claims 22-26 and 33 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Anand. Claims 34, 36, and 38 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Anand in view of U.S. Patent Number 5,350,940 by Rona (hereinafter "Rona").

Claims 1, 5, 7, 15, 16, 18, 19, 21, and 26-38 have been amended. Claim 20 has been canceled.

Claims 5, 7, 13, 15, 20, and 26 stand rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicant has amended Claims 5, 7, 15, 20, and 26 to improve the inherent antecedent basis for some of the limitations in those claims as well as to redefined an existing limitation without narrowing the scope of the claim. Applicants reserve all rights with respect to the application of the doctrine equivalents. Applicants add the following explanation to clear up the objection to claim 13. Claim 13 includes the wording that the logic is configured to do both compression of bits and decompression of bits. Thus, the processor of claim 1 and its dependent claim 13 respectively, contains logic that can both compress bits and decompress bits.

Therefore, the logic of claim 13 is referring to both decompression logic and compression logic.

In accordance with PTO guidelines, applicants in general traverse the inherent disclosure of the limitations in the claims and request specific documentation, via a prior art document or a signed declaration by the examiner, of these known facts in the art.

Applicants assert that independent claim 1 is not obvious under 35 U.S.C. § 103(a) in view of the combination of Anand and Weiss.

Claim 1 states:

> An apparatus, comprising:
> two or more memories having one or more redundant components associated with each memory, the one or more redundant components include at least one redundant column of memory cells;
> a first processor containing redundancy allocation logic to execute one or more repair algorithms to generate a repair signature for each memory; and
> a repair data container to store an actual repair signature for each memory having one or more defective memory cells detected during fault testing and a dummy repair signature for each memory with no defective memory cells.

In contrast to the Office Actions initial assessment, Weiss does not disclose a single on chip processor coupled and configured to repair multiple discrete memory cores. Rather, Weiss repeatedly discusses a processor coupled to a single memory block/core with multiple segments within that single memory block. Accordingly, Weiss discloses:

> A method of repairing a memory block, said method comprising: detecting a defect within a segment of a memory block having multiple segments; (Weiss Col. 14 Lns. 59-62) (Emphasis added)

> A computer system comprising:
> a processor for executing instructions;
> a repairable memory structure accessible by said processor, said repairable

> memory structure comprising multiple segments of memory cells, wherein at least one of said multiple segments is repairable in that it has associated therewith repair circuitry controllable to reroute a memory access from a defective memory cell of the at least one repairable segment to a non-defective memory cell; (Weiss Col. 16 Lns. 11-20) (Emphasis added)

Also, neither does Anand disclose a single on-chip processor coupled and configured to repair multiple discrete memory cores. Rather, Anand discusses that the testing and fuse programming happens during fabrication of the integrated circuit (IC) and typically that occurs with an external testing unit and not an on-chip test processor. See columns 1 and 2 of Anand. Anand also teaches the IC field of art's concern about the limited area available on a chip to place components. Thus, suggesting the general resistance of that field of art to place a test processor on the chip when an external test unit could also test the memories during the fabrication process. Accordingly, Anand states:

> Fuses 12 are arranged in a block isolated from the fuse-programmable macros, in order to overcome the obstacles associated with placing fuses such as interference with interconnect points, inefficient use of die area due to guard rings, laser-programmable fuses or e-fuses requiring the entire layer stack for implementation, et cetera. (Anand Col. 3 Lns. 43-51) (Emphasis added)

Thus, the combination of Anand and Weiss would lack an on-chip processor testing multiple memory cores.

As discussed above, Anand also teaches the IC field of art's concern about the limited area available on a chip to place components. Therefore, Anand teaches that in the field of ICs the concept of adding both an on-chip processor and an on-chip repair container in the limited available space on a chip would not be a mere integrating of a plurality of pieces. Since neither prior art document contains language suggesting this combination, and in fact Anand teaches away from this concept, the combination with

Weiss is improper under the law governing 35 USC 103 combinations. Additionally, even if the combination was proper, the combination would still lack teaching or suggesting a single on chip processor coupled and configured to repair multiple discrete memory cores and then configured to store those repair signature in an on-chip repair data container. Therefore, for both reasons, independent claim 1 is patently distinct over Anand and Weiss.

Given that claims 2-15 depend from and include the limitations of claim 1, applicants submit that claims 2-15 are not obvious under 35 U.S.C. § 103(a) in view of the combination of Anand and Weiss.

Likewise, independent claims 16, 35 and 37 and their respective dependent claims contain similar limitations but not identical to those discussed for claim 1. Thus, independent claims 16, 35 and 37 and their respective dependent claims are patentably distinct from Anand and Weiss for their own reasons but similar to the above arguments.

In light of the above discussion, Anand and Weiss do not disclose two on-chip processors, each coupled and configured to repair multiple discrete memory cores and then configured to store those repair signature in a single on-chip repair data container. Thus, independent claims 22 and 33 and their respective dependent claims are patentably distinct from Anand and Weiss for their own reasons but similar to the above arguments.

Claims 27, 29, 30, and 32 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Anand. Claims 27, 28, 30, 31, 35, and 37 stand rejected under 35 U.S.C. § 103(a) as being anticipated by Weiss in view of Anand.

Applicants assert that independent claim 27, as amended, is not obvious under 35 U.S.C. § 103(a) in view of the combination of Anand and Weiss. Applicants also assert that independent claim 27, as amended, is not anticipated by Anand.

Claim 27, as amended, states:

> A method, comprising:
> composing a repair signature for two or more memory cores on every cycle a device containing the two or more memory cores is initialized;
> sending the repair signature for each memory core to be stored in non-volatile fuses; and
> decompressing the repair signature for each memory core to send reconfiguration data to the two or more memory cores.

Anand discusses that the testing and fuse programming is determined during fabrication of the IC and the redundancy allotation as a result of the fuse program is implemented the first time when the IC is initialized during operation. See the background section columns 1 and 2. Additionally, Anand states:

> The present invention concerns the manner in and means by which control data for controlling the customization and/or repair of integrated circuit 10 is accomplished. Fuses 12 are arranged in a block isolated from the fuse-programmable macros, in order to overcome the obstacles associated with placing fuses such as interference with interconnect points, inefficient use of die area due to guard rings, laser-programmable fuses or e-fuses requiring the entire layer stack for implementation, et cetera. The fuse data contains compressed information that is decompressed by decompressor 14 to produce the control data for repairing or customizing fuse-programmable macros 16. Shift registers 18 within the macros are arranged in chains to allow serial clocking of decompressed control data received from decompressor 14, so that at initialization, the control data is propagated to fuse-programmable macros 16. After initialization, the functional logic implemented by fuse-programmable macros 16 will be configured for operation of integrated circuit 10. (Anand Col. 3 Lns. 51-60)

Thus, Anand is very clear that no subsequent BIST testing and augmented repair for newly found defects while the device containing the IC is in a customer's hands and

in operation was ever taught or suggested in Anand. As discussed above, Weiss does not teach or suggest having an on-chip processor to BIST test that generates a repair signature on every cycle a device is initialized. Claim 27 states "composing a repair signature for two or more memory cores on every cycle a device containing the two or more memory cores is initialized." Thus, Anand by itself or in combination with Weiss does not disclose the limitations in claim 27. Therefore, independent claim 27 is patently distinct over Anand and Weiss.

Likewise, independent claim 30 and its respective dependent claims contain similar limitations but not identical to those discussed for claim 27. Thus, independent claim 30 and its respective dependent claims are patentably distinct from Anand and Weiss for their own reasons but similar to the above arguments.

Claims 34, 36, and 38 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent Number 66,577,156 by Anand in view of Rona. However, Rona contains the same deficiencies discussed for Anand and Weiss. Thus, Claims 34, 36, and 38 are patentably distinct from Anand and Rona for their own reasons but similar to the above arguments.

Conclusion

It is respectfully submitted that in view of the amendments and remarks set forth herein, the rejections and objections have been overcome. An Information Disclosure Statement is also submitted with this amendment. Applicants reserve all rights with respect to the application of the doctrine equivalents. If there are any additional charges, please charge them to our Deposit Account No. 02-2666. Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,
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